ABSTRACT OF THE DISCLOSURE

A memory cell with reduced short channel effects is described. A source region and a drain region are formed in a semiconductor substrate. A trench region is formed between the source region and the drain region. A recessed channel region is formed below the trench region, the source region and the drain region. A gate dielectric layer is formed in the trench region of the semiconductor substrate above the recessed channel region and between the source region and the drain region. A control gate layer is formed on the semiconductor substrate above the recessed channel region, wherein the control gate layer is separated from the recessed channel region by the gate dielectric layer.

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